

Form PTO 1449  
Rev 7-80U.S. Dept of Commerce  
Patent & Trademark Off.Atty. Docket No.  
93-C-032C3Serial No.  
09/007,668

#21/2

Applicant  
Alex Kalnitsky, et al.Filing Date  
January 15, 1998Group  
2811LIST OF PRIOR ART CITED BY APPLICANT  
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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
AA	4,253,907	3/81	Parry et al.	156/643	
AB	4,354,896	10/82	Hunter	156/643	
AC	4,384,938	5/83	Desilets et al.	204/298	
AD	4,654,112	3/87	Douglas et al.	156/643	
AE	4,657,628	4/87	Holloway et al.	156/643	
AF	4,660,278	4/87	Teng	29/576	
AG	4,676,867	6/87	Elkins et al.	257/752	
AH	4,707,218	11/87	Giammarco et al.	156/643	
AI	4,721,548	1/88	Morimoto	156/657	
AJ	4,755,476	7/88	Bohm et al.	437/31	
AK	4,792,534	12/88	Tsuji et al.	437/229	

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## FOREIGN COUNTRIES

	DOC. NO.	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION
AL	410244	1/91	Germany		
AM	8901236	5/92	Great Britain		

## OTHER PRIOR ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGE, ETC.)

AN	"Advantages of Using Spin on Glass Layer in Interconnection Dielectric Planarization", Microelectronic Engineering, Vol. 5 (1986).
AO	"Doped Silicon Oxide Deposition by Atmospheric Pressure and Low Temperature Chemical Vapor Deposition Using Tetraethoxysilane and Ozone", Fujino et al., J. Electrochem. Society, Vol. 138, No. 10, p. 3019 Oct 1991
AP	"Polysilicon Planarization Using Spin-On Glass", S. Ramaswami and A. Nagy, J. Electrochem. Soc., Vol. 139, No. 2, p. 591 (1992).

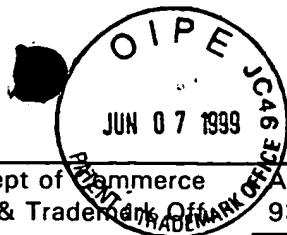
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6	BM	60-58635	4/85	Japan	

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6	BN	"Three 'Low Dt' Options for Planarizing the Premetal Dielectric on an Advanced Double Poly BiCMOS Process", by W. Dauksher, M. Miller, and C. Tracey, J. Electrochem. Soc., Vol. 139, No. 2, p. 532 (1992)/			
6	BO	"The Effect of Plasma Cure Temperature on Spin-On Glass", by H. Namatsu and K. Minegishi, J. Electrochem. Soc., Vol. 140, No. 4, p. 140 (1991).			
6	BP	"Hot-Carrier Aging of the MOS Transistor in the Presence of Spin-On Glass as the Interlevel Dielectric", by N. Lifschitz and G. Smolinsky, IEEE Electron Device Letters, Vol. 12, No. 3, p. 140 (1991).			

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SN	CA	5,117,273	5/92	Stark et al.	357/54
	CB	5,158,910	10/92	Cooper et al.	437/195
	CC	5,166,088	11/92	Ueda et al.	437/47
	CD	5,244,841	9/93	Marks et al.	437/228
	CE	5,250,472	10/93	Chen et al.	437/231
	CF	5,266,525	11/93	Morozumi	437/195
	CG	5,310,720	5/94	Shin et al.	437/231
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SN	CK	61-26240	2/86	Japan	
SN	CL	62-106645	4/87	Japan	
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SN	CO	"Reactive Ion Etching", by B. Gorowitz and R. Saia, 8 VLSI Electronics, 297ff (1984).			
SN	CP	Patent Abstracts of Japan, Vol. 15, No. 348 (E-1107) 4 Sept. 1991 & JP-A-31 33 131 (Mitsubishi Electric Corp.) 6 June 1991.			

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EXAMINER INITIAL	DOC. NO.	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION
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DG	2083948A	3/82	Europe		
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DI	IBM Technical Disclosure Bulletin, Vol. 30, No. 8, p. 252, January 1988.
DJ	IBM Technical Disclosure Bulletin, Vol. 29, No. 3, p. 1328, August 1986.
DK	"A New Technology for Oxide Contact and Via Etch", by Pete Singer, Semiconductor International, p. 36 (1993).
DL	Handbook on Semiconductors, (ed. C. Holson), Vol. 4, p. 208 (1981).
DM	"Etching Applications and Trends of Dry Etching", Ephrath et al., Semiconductor Technology and Computer Systems, Ch. 2, p. 26. 1991
DN	VLSI Electronics Microstructure Science, Vol. 8, ed. Norman Einspruch, p. 298 (1984).
DO	"Plasma Etch Anisotropy", C.B. Zarowin, J. Electrochem. Soc., Solid-State Science and Technology, p. 1144 (1983).
DP	"A Super Self-Aligned Source/Drain MOSFET," Lau et al., IEDM, p. 358 (1987).
DQ	"A Margin-Free Contact Process Using an Al3O3 Etch-Stop Layer for High Density Devices", Fukase et al., IEDM, p. 837 (1992).
DR	<del>VLSI Fabrication Principles, Silicon and Gallium Arsenide, by Sarab K. Ghanti</del>
DS	Research Disclosure No. 282, October 1987; Havant GB page 608, "Spin on Glass Insulator Enhancement".

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